FIG. 1

	EAST				WEST			
	RCV		TRMT		TRMT		RCV	
E ⇒ W	S1	D1	S2	D2	S3	D3	S4	D4
W ⇒ E	D1	S1	D2	S2	D3	S3	D4	S4

Sx : Source Node ID / Dx : Destination Node ID (4 bits each)

FIG. 2

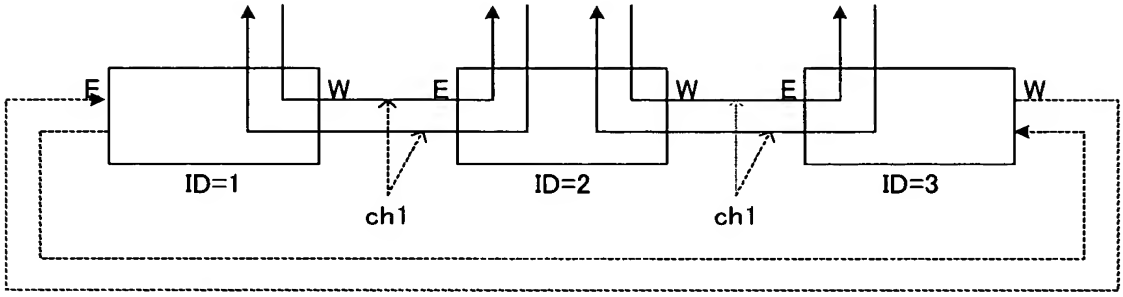


FIG. 3

	EAST				WEST			
	RCV		TRMT		TRMT		RCV	
E ⇒ W	1	2	2	1	2	3	3	2
W ⇒ E	2	1	1	2	3	2	2	3

FIG. 4A

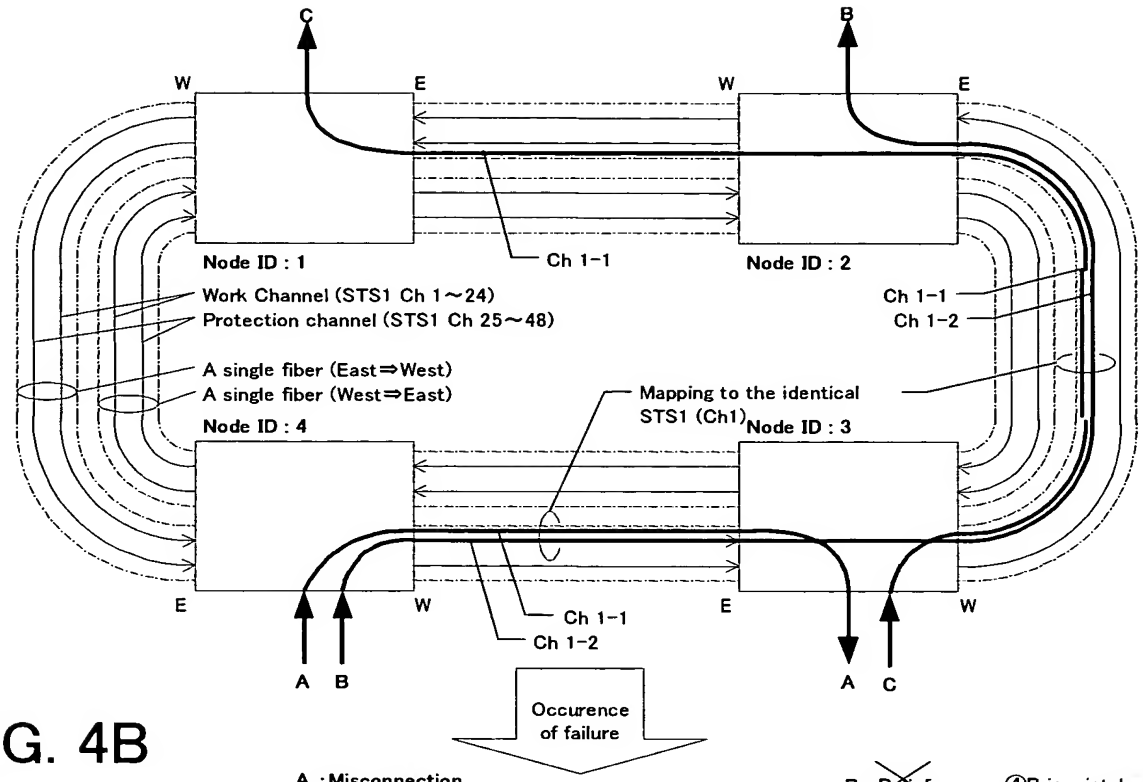

C
B
W
E
W
E
Node ID : 1
Ch 1-1
Node ID : 2
Work Channel (STS1 Ch 1～24)
Protection channel (STS1 Ch 25～48)
Ch 1-1
Ch 1-2
A single fiber (East⇒West)
A single fiber (West⇒East)
Mapping to the identical STS1 (Ch1)
Node ID : 4
Node ID : 3
E
W
E
W
Ch 1-1
Ch 1-2
A
B
A
C
Occurence of failure

FIG. 4B

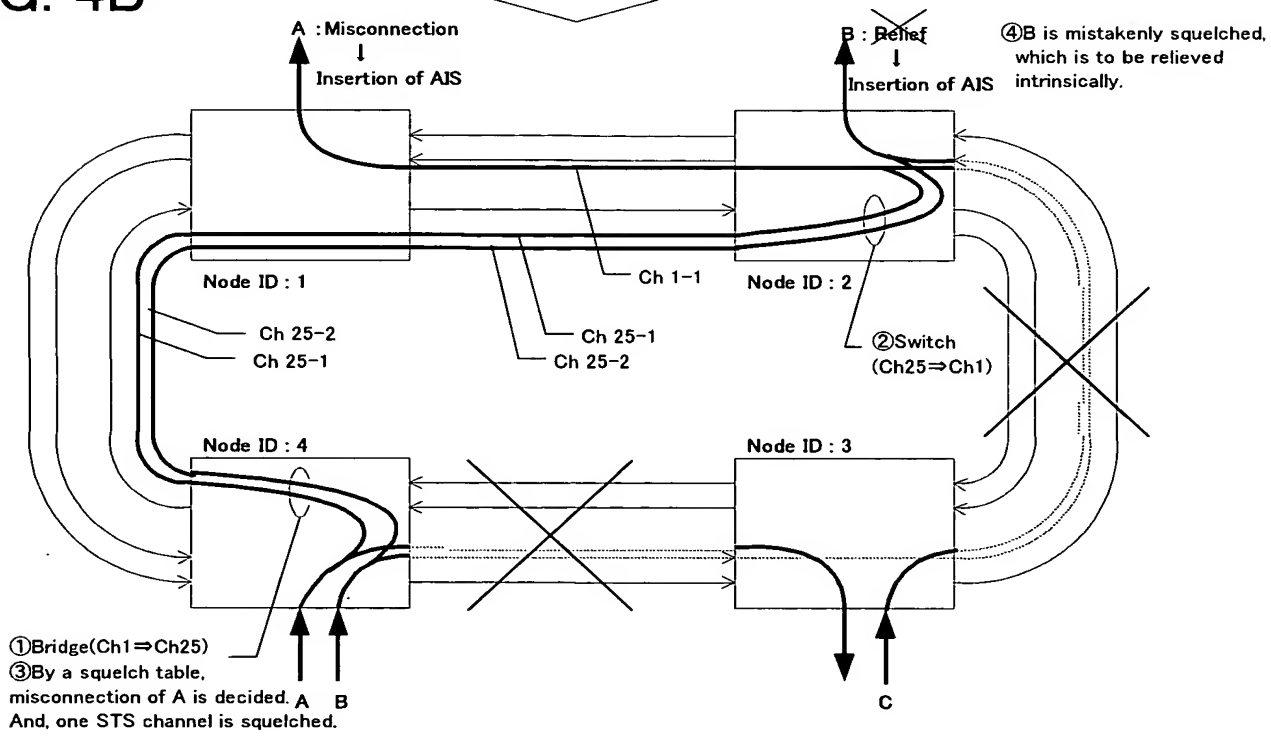

A : Misconnection
Insertion of AIS
B : Relief
Insertion of AIS
④B is mistakenly squelched, which is to be relieved intrinsically.
Node ID : 1
Ch 1-1
Node ID : 2
Ch 25-2
Ch 25-1
Ch 25-1
Ch 25-2
②Switch (Ch25⇒Ch1)
Node ID : 4
Node ID : 3
①Bridge(Ch1⇒Ch25)
③By a squelch table, misconnection of A is decided. And, one STS channel is squelched.
A
B
C

FIG. 5A

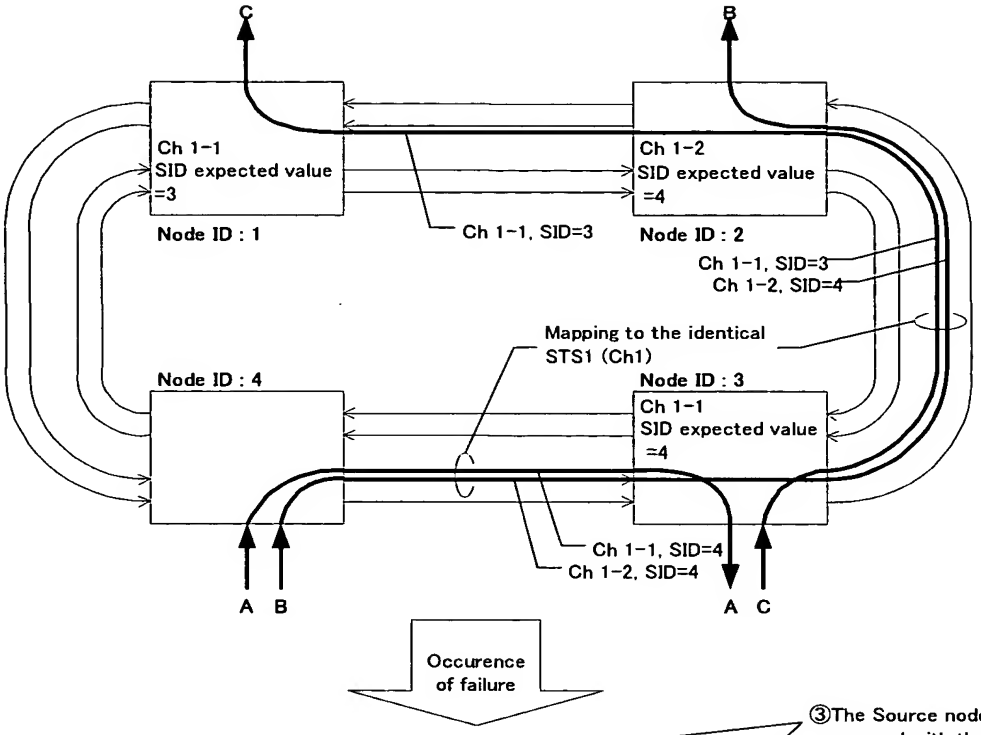
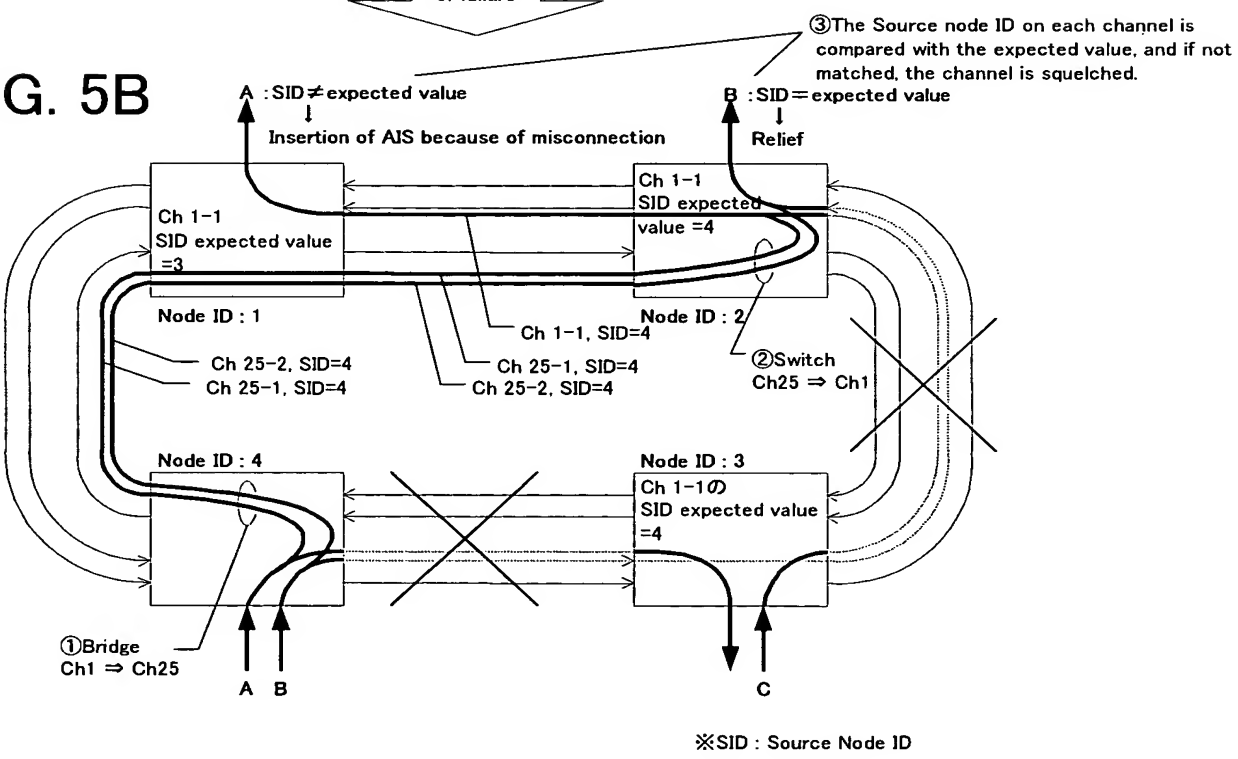


FIG. 5B



※SID : Source Node ID

FIG. 6A

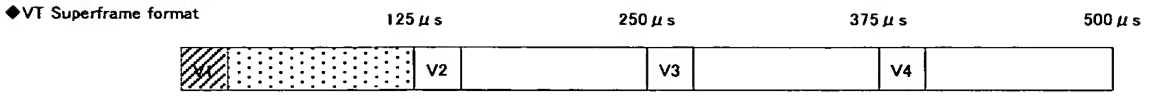


FIG. 6B

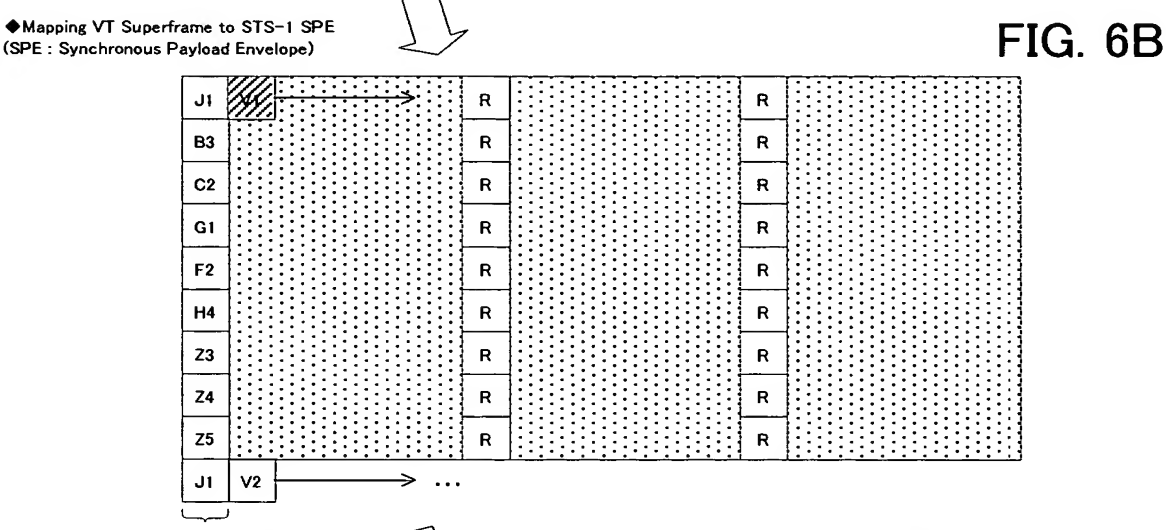


FIG. 6C

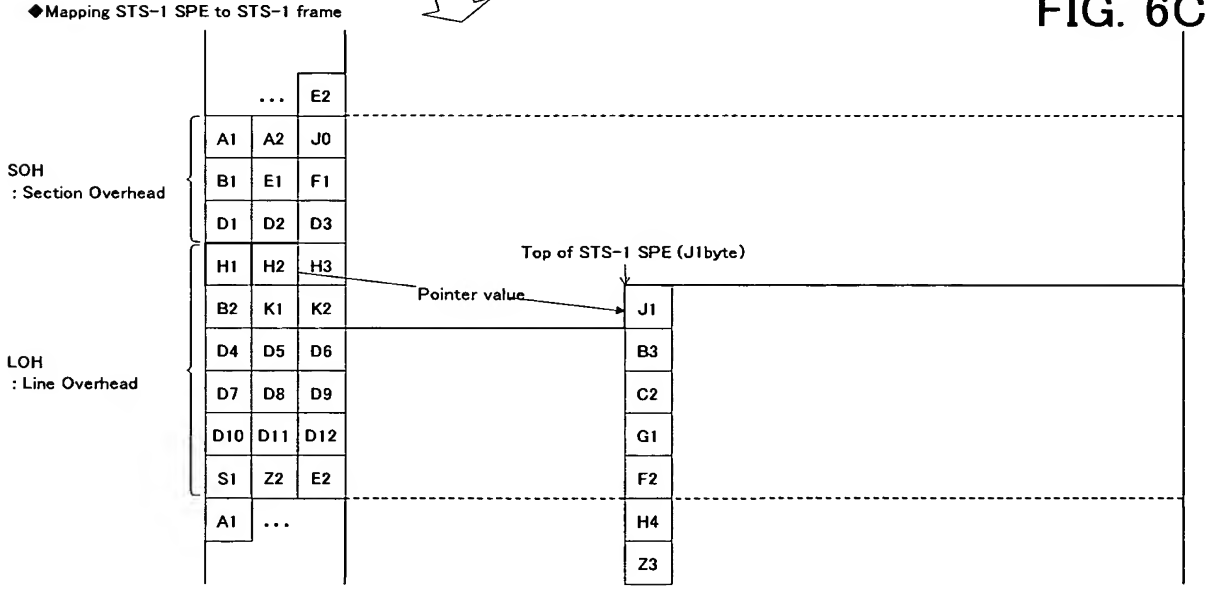


FIG. 7

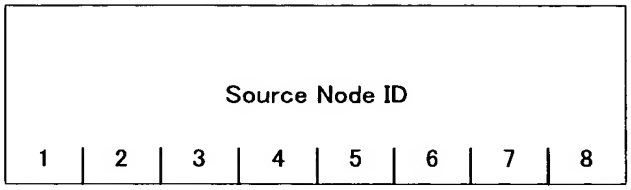


FIG. 8

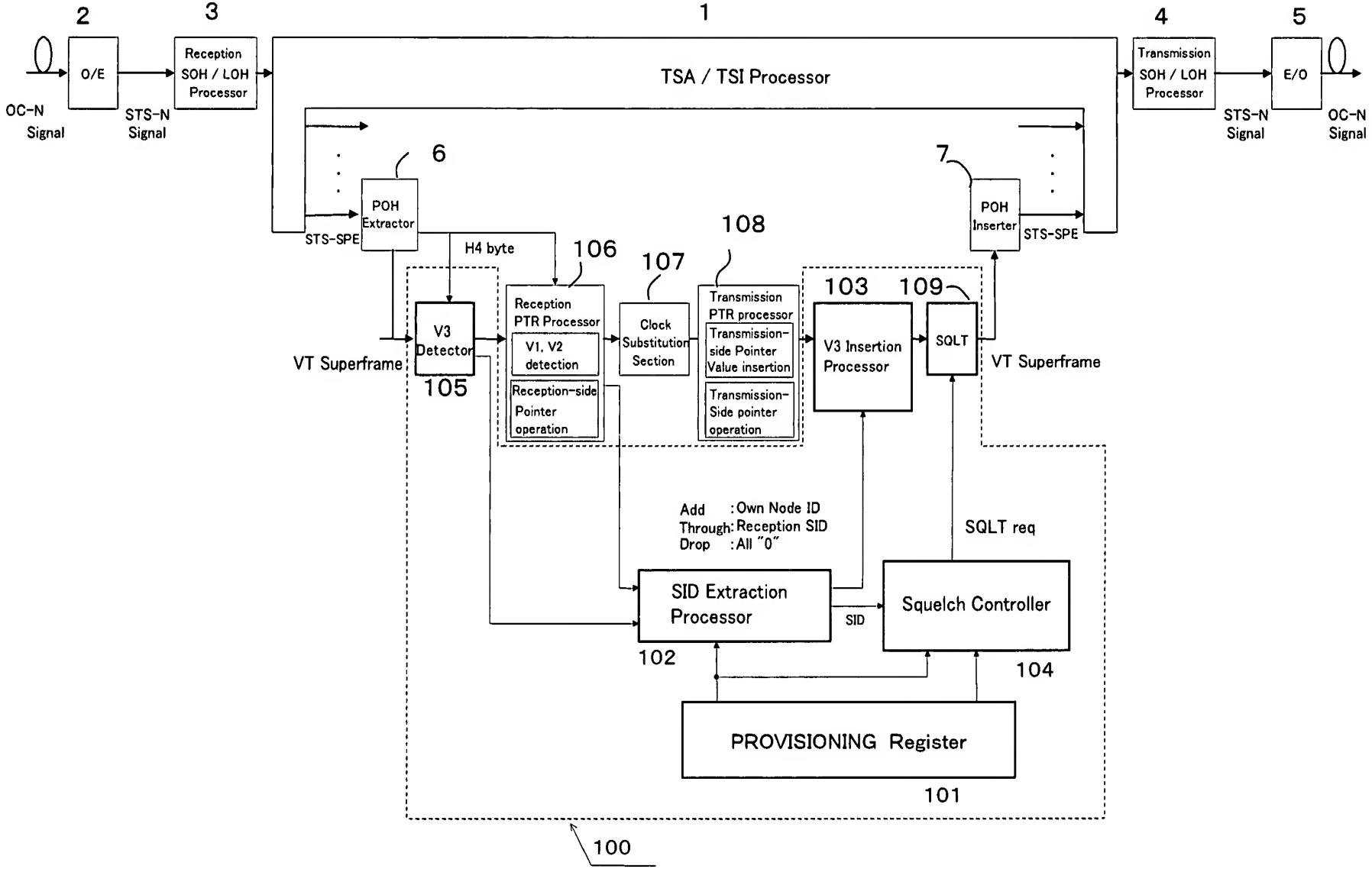

2
3
1
4
5
O/E
Reception SOH / LOH Processor
TSA / TSI Processor
Transmission SOH / LOH Processor
E/O
OC-N Signal
STS-N Signal
STS-N Signal
OC-N Signal
6
7
POH Extractor
POH Inserter
STS-SPE
STS-SPE
H4 byte
106
107
108
103
109
V3 Detector
Reception PTR Processor
V1, V2 detection
Reception-side Pointer operation
Clock Substitution Section
Transmission PTR processor
Transmission-side Pointer Value insertion
Transmission-Side pointer operation
V3 Insertion Processor
SQLT
VT Superframe
VT Superframe
105
Add : Own Node ID
Through: Reception SID
Drop : All "0"
SQLT req
SID Extraction Processor
SID
Squelch Controller
102
104
PROVISIONING Register
101
100

FIG. 9

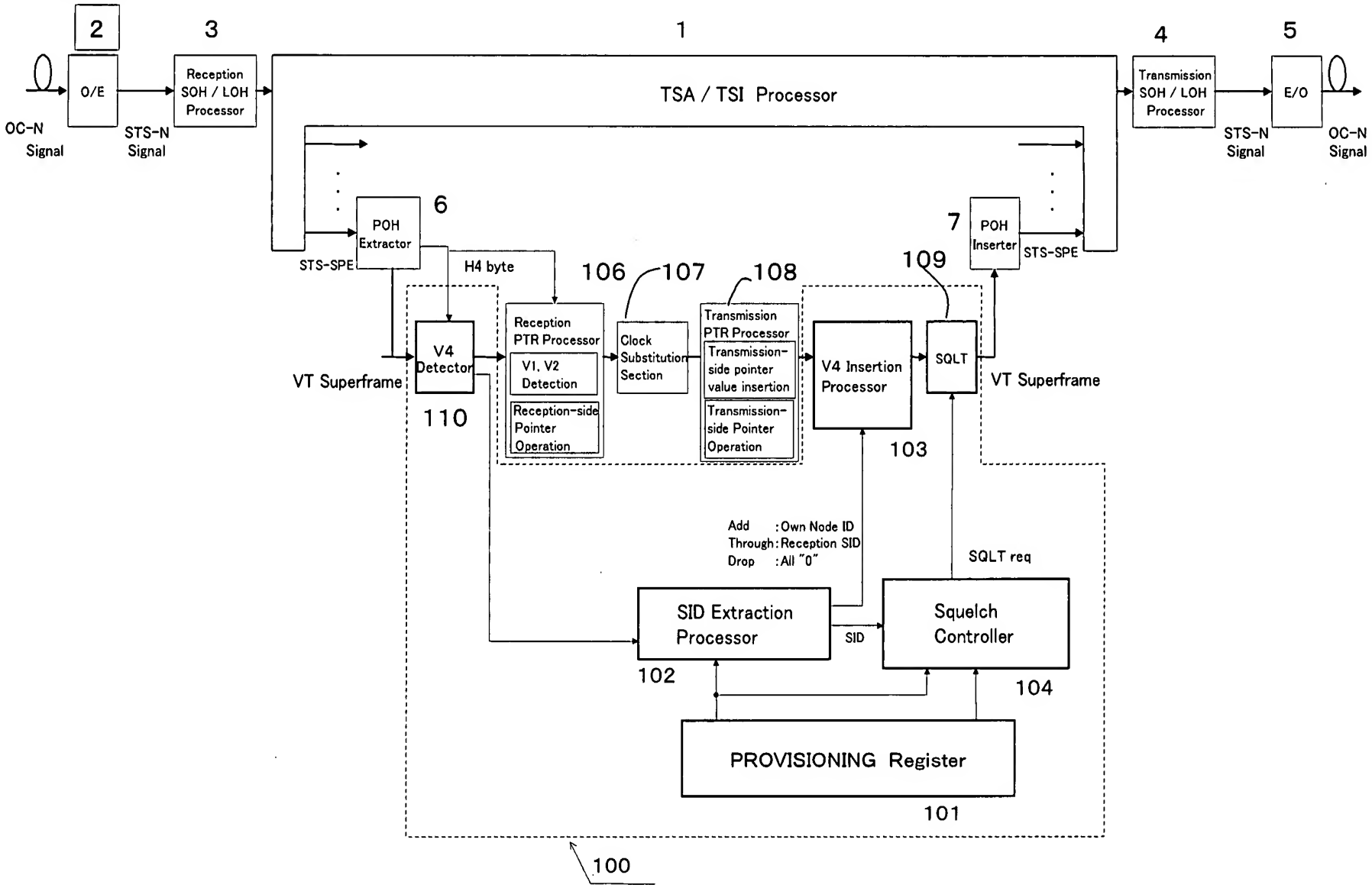

2
3
1
4
5
O/E
Reception SOH / LOH Processor
TSA / TSI Processor
Transmission SOH / LOH Processor
E/O
OC-N Signal
STS-N Signal
STS-N Signal
OC-N Signal
6
POH Extractor
7
POH Inserter
STS-SPE
STS-SPE
H4 byte
106
107
108
109
Reception PTR Processor
V1, V2 Detection
Reception-side Pointer Operation
Clock Substitution Section
Transmission PTR Processor
Transmission-side pointer value insertion
Transmission-side Pointer Operation
V4 Insertion Processor
SQLT
VT Superframe
VT Superframe
V4 Detector
110
103
Add : Own Node ID
Through : Reception SID
Drop : All "0"
SQLT req
SID Extraction Processor
SID
Squelch Controller
102
104
PROVISIONING Register
101
100

FIG. 10A

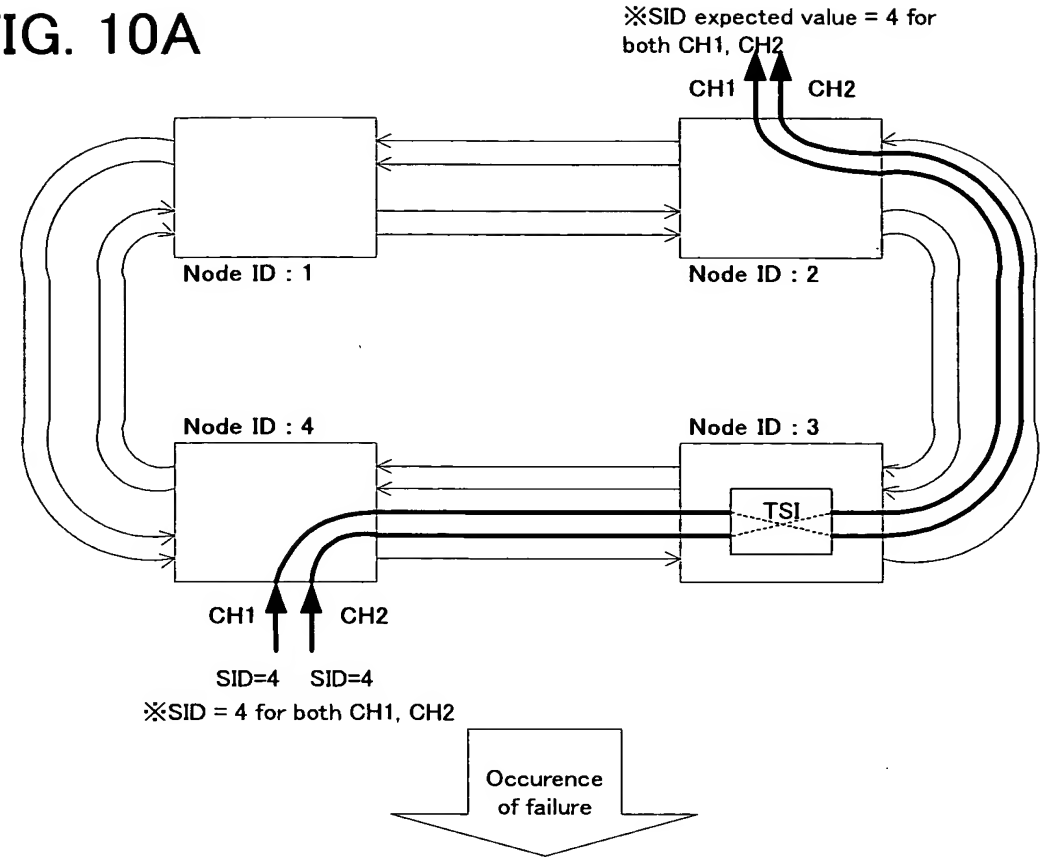


FIG. 10B

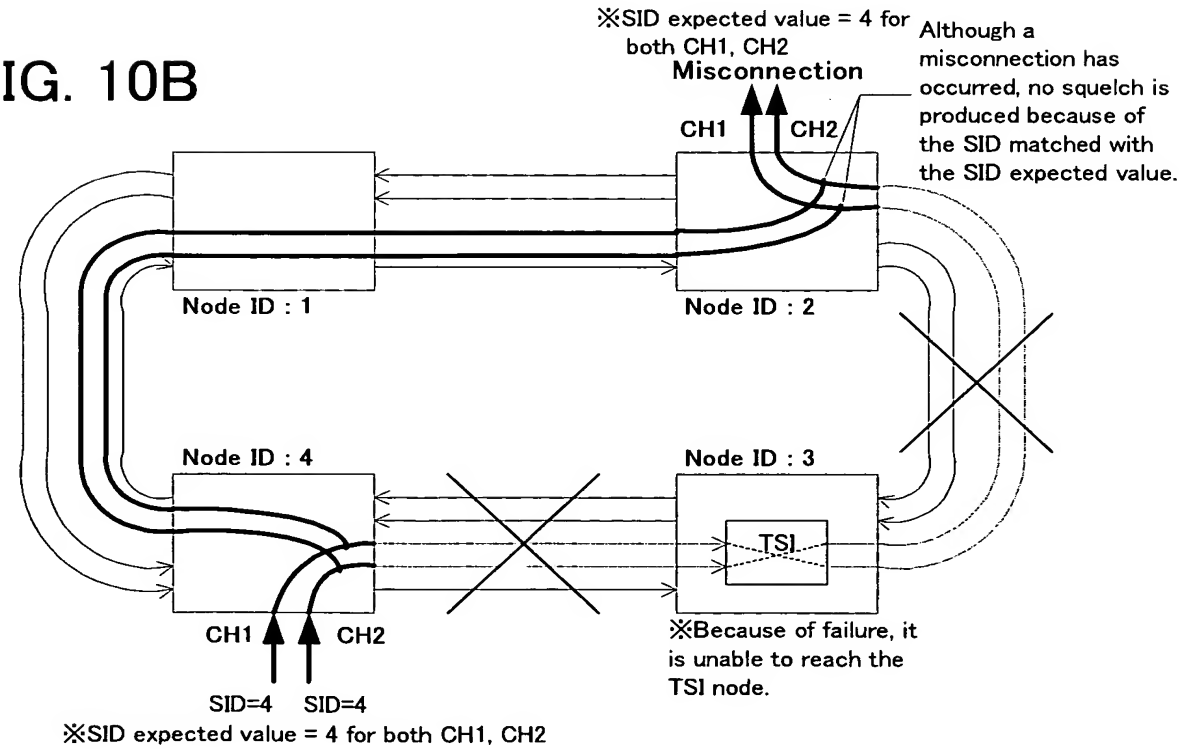


FIG. 11A

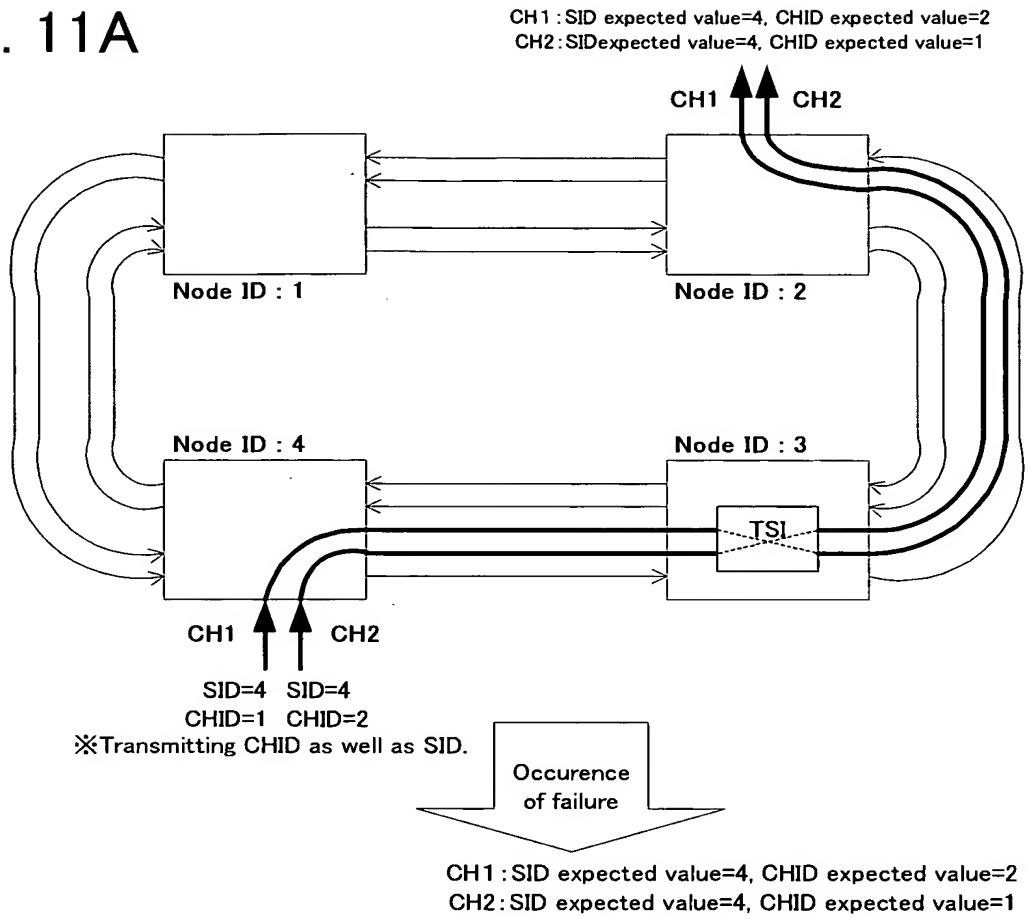


FIG. 11B

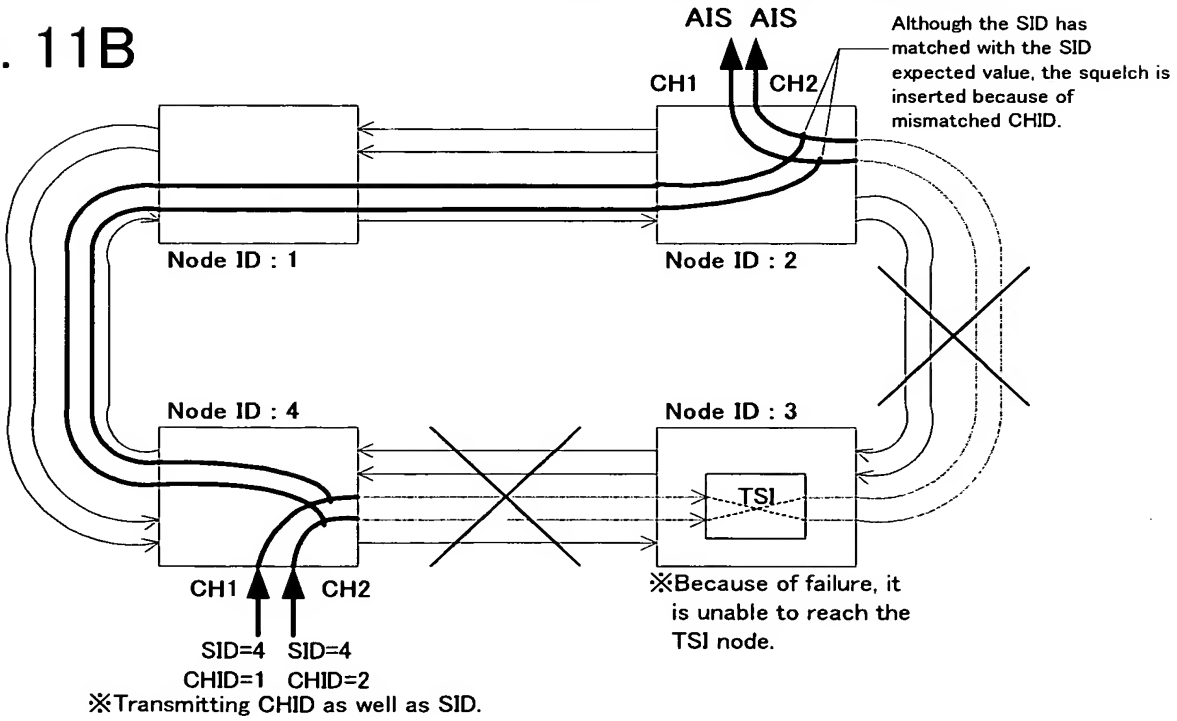


FIG. 12A

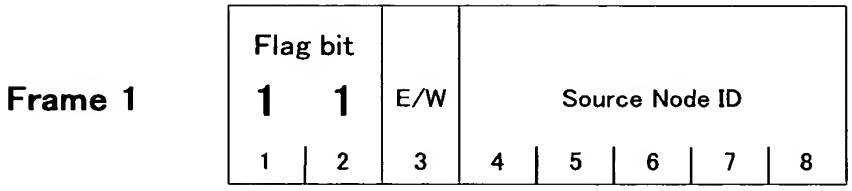


FIG. 12B

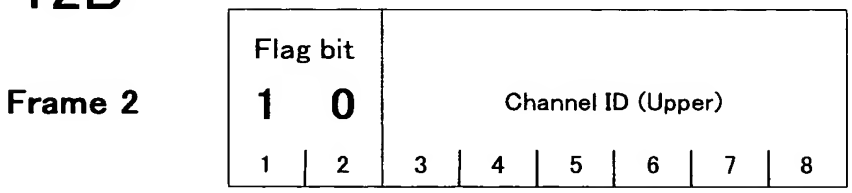


FIG. 12C

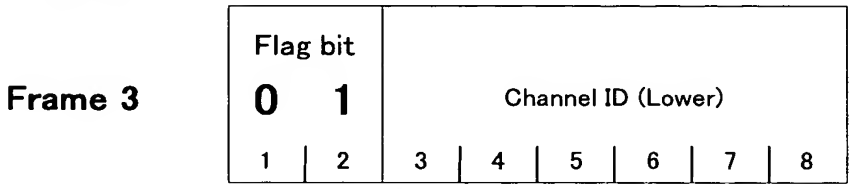


FIG. 13 A

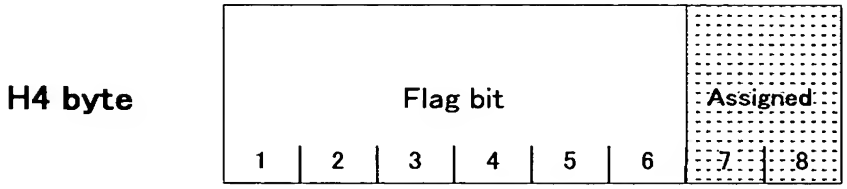


FIG. 13B

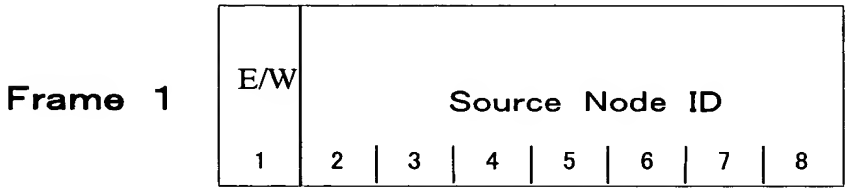


FIG. 13C

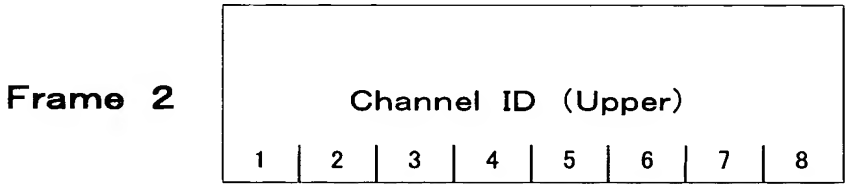


FIG. 13D

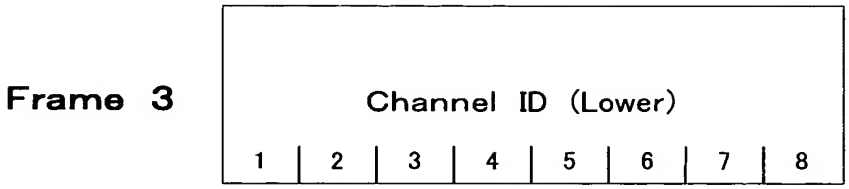


FIG. 14

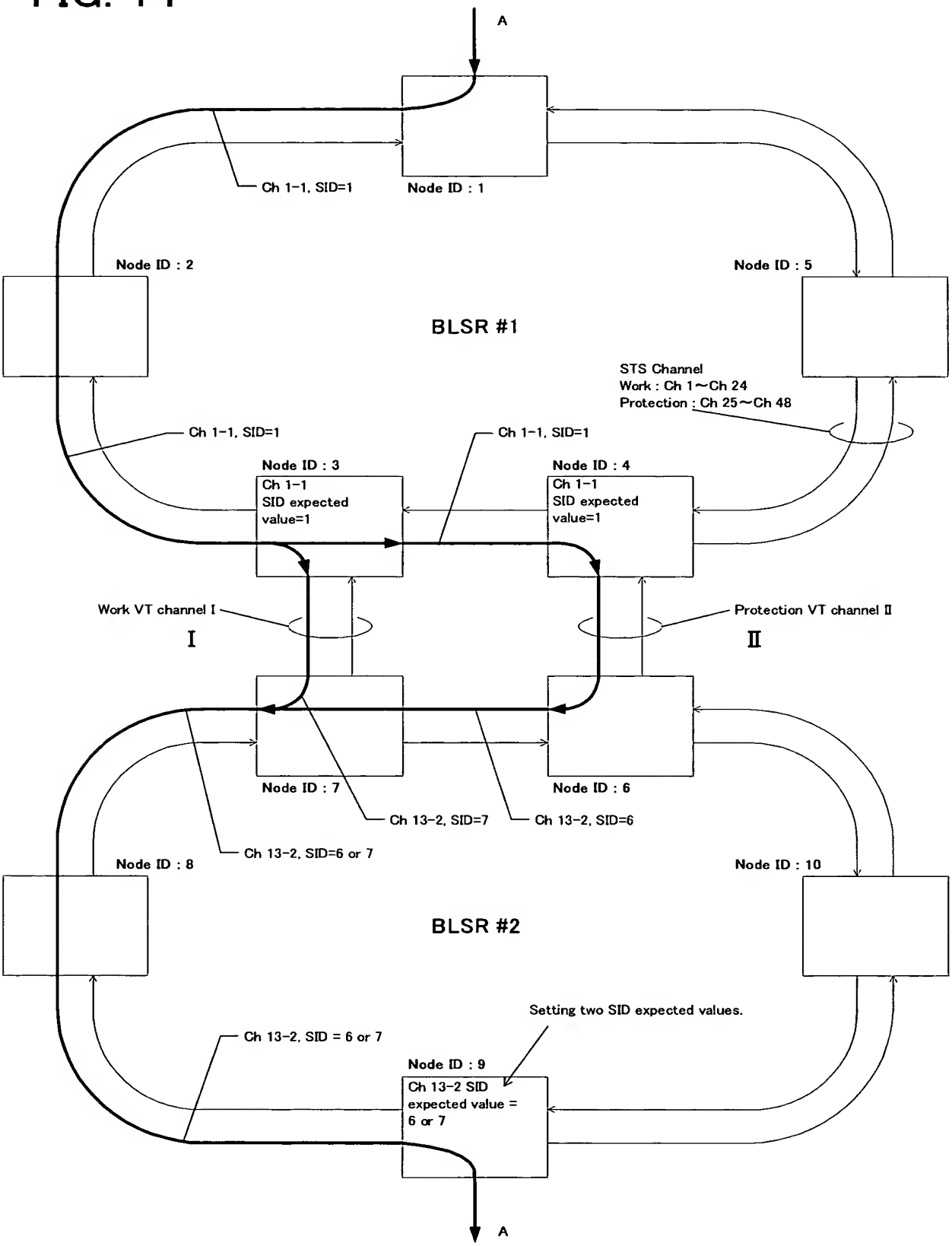
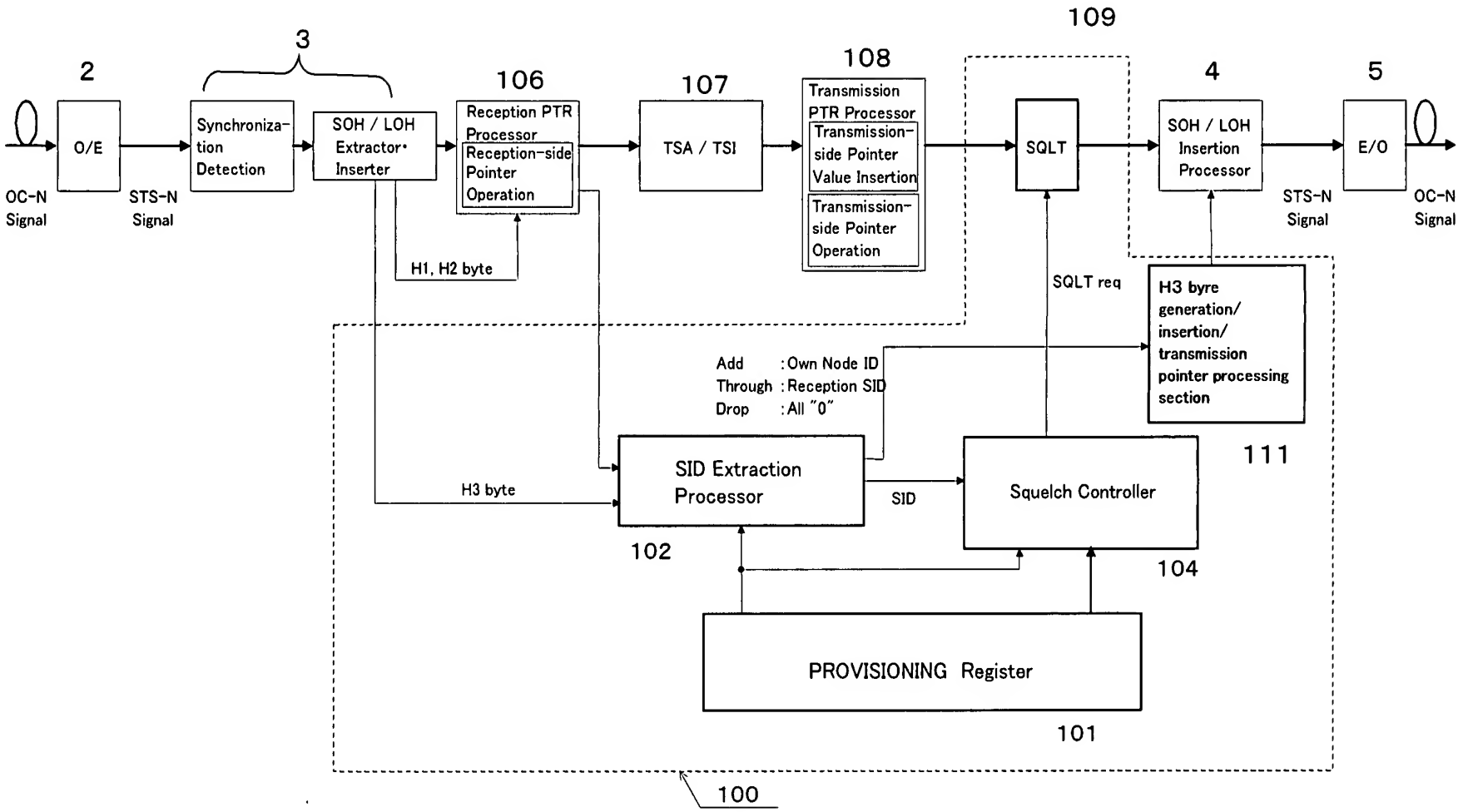

A
Ch 1-1, SID=1
Node ID : 1
Node ID : 2
Node ID : 5
BLSR #1
STS Channel
Work : Ch 1~Ch 24
Protection : Ch 25~Ch 48
Ch 1-1, SID=1
Ch 1-1, SID=1
Node ID : 3
Ch 1-1
SID expected
value=1
Node ID : 4
Ch 1-1
SID expected
value=1
Work VT channel I
I
Protection VT channel II
II
Node ID : 7
Node ID : 6
Ch 13-2, SID=7
Ch 13-2, SID=6
Ch 13-2, SID=6 or 7
Node ID : 8
Node ID : 10
BLSR #2
Setting two SID expected values.
Ch 13-2, SID = 6 or 7
Node ID : 9
Ch 13-2 SID
expected value =
6 or 7
A

FIG. 15


109
3
2
108
106
107
4
5
Transmission PTR Processor
Transmission-side Pointer Value Insertion
Transmission-side Pointer Operation
Reception PTR Processor
Reception-side Pointer Operation
O/E
Synchroniza-tion Detection
SOH / LOH Extractor• Inserter
TSA / TSI
SQLT
SOH / LOH Insertion Processor
E/O
OC-N Signal
STS-N Signal
STS-N Signal
OC-N Signal
H1, H2 byte
SQLT req
H3 byre generation/ insertion/ transmission pointer processing section
111
Add : Own Node ID
Through : Reception SID
Drop : All "0"
SID Extraction Processor
H3 byte
SID
Squelch Controller
102
104
PROVISIONING Register
101
100